

Inventor: Wendell P. Noble

Title: Semiconductor Processing Methods of Forming Integrated Circuitry, Forming Conductive Lines, Forming a Conductive Grid, Forming a Conductive Network, Forming an Electrical Interconnection to a Node Location, Forming an Electrical Interconnection with a Transistor Source/Drain Region, and Integrated Circuitry

Assignee: Micron Technology, Inc.

INFORMATION DISCLOSURE STATEMENT

PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

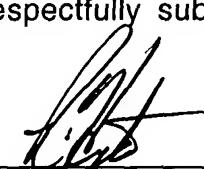
The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 10/227,500, filed August 22, 2002. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 7/29/03

By:



Robert C. Hyta
Reg. No. 46,791

EV317134177

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				ATTY. DOCKET NO. M122-2378	SERIAL NO. Filed Herewith		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Wendell P. Noble			
				FILING DATE Filed Herewith		GROUP Unassigned	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,539,229	07/96	Noble, Jr., et al.			
	AB	5,214,603	05/93	Dhong, et al.			
	AC	4,604,162	08/86	Sobczak			
	AD	5,391,911	02/95	Beyer, et al.			
	AE	5,763,931	06/98	Sugiyama			
	AF	5,599,724	02/97	Yoshida			
	AG	5,846,854	12/98	Giraud, et al.			
	AH	5,011,783	04/91	Ogawa, et al.			
	AI	4,700,461	10/87	Choi, et al.			
	AJ	5,608,248	03/97	Ohno			
	AK	6,091,129	07/00	Cleaves			
	AL	6,004,865	12/99	Horiuchi, et al.			
	AM	5,831,305	11/98	Kim			
	AN	6,117,760	09/00	Gardner, et al.			
	AO	6,373,138	04/02	Noble			
	AP	6,274,919	08/01	Wada			
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes
	AQ	0 720 221 A1	07/96	EPO			
	AR						
	AS						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AT		Davari et. al., "A Variable-Size Shallow Trench Isolation (STI) Technology With Diffused Sidewall Doping For Submicron CMOS,"				
			<i>IEDM Technical Digest</i> , International Electron Devices Meeting, San Francisco, CA, Dec. 11-14, 1988, pp. 92-95.				
	AU		Bakeman et. al., "A High Performance 16-Mb Dram Technology," <i>1990 Symposium on VLSI Technology Digest of Technical Papers</i> ,				
			1990 VLSI Technology Symposium, Honolulu, HI, June 4-7, 1990, pp. 11-12.				
EXAMINER			DATE CONSIDERED				
<small>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>							

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U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,241,211	08/93	Tashiro			
	AB						
	AC						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
	AP						Yes No
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AS		Suma et. al., "An SOI-DRAM With Wide Operating Voltage Range by CMOS/SIMOX Technology," <i>IEEE Journal of Solid-State Circuits</i> , November 1994, pp. 1323-1329.				
			Kuge et. al., "SOI-DRAM Circuit Technologies For Low Power High Speed Multigiga Scale Memories", <i>IEEE Journal of Solid-State Circuits</i> , April 1996, pp. 586-591.				
			Y. Kohyama et al., "Buried Bit Line Cell for 64MB DRAMs," IEEE, 1990 Symposium on VLSI Technology, pp. 17, 18.				
			IBM Technical Disclosure Bulletin, "Buried Stud That Eliminates Substrate and Well Contact Requirements", Vol. 39, Pub No. 6, June 1996.				
			Takahiro Onai et al., "SEPIA: A New Isolation Structure for Soft-Error-Immune LSI's," 1993 IEEE, 3 pages.				
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							